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(54) Abstract Title
Method of analyzing a semiconductor ingot

(57) A method of analyzing crystal defects of bare wafers prepared by cutting a single crystal ingot grown by the Czochralski method comprises the steps of a) sampling wafers with respect to their positions in the ingot after forming wafers from a plurality of ingots formed under the same crystal growth conditions ; b) analyzing the crystal defects of some of the wafers in the as-grown state; c) selecting some other wafers, carrying out a thermal treatment process on the wafers under the same temperature conditions as the thermal treatment process of a semiconductor device fabrication process and analyzing the crystal defects; d) selecting some other wafers, carrying out an accelerated thermal treatment on the wafers, and analyzing the crystal defects of the wafers, and e) estimating the state of the crystal defects with respect to the position in the ingots based on the above analysis results. The defects concerned include OP (oxygen precipitate), COP (crystal originated particle), D-defects and heavy metal defects.

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FIG. 1
(PRIOR ART)

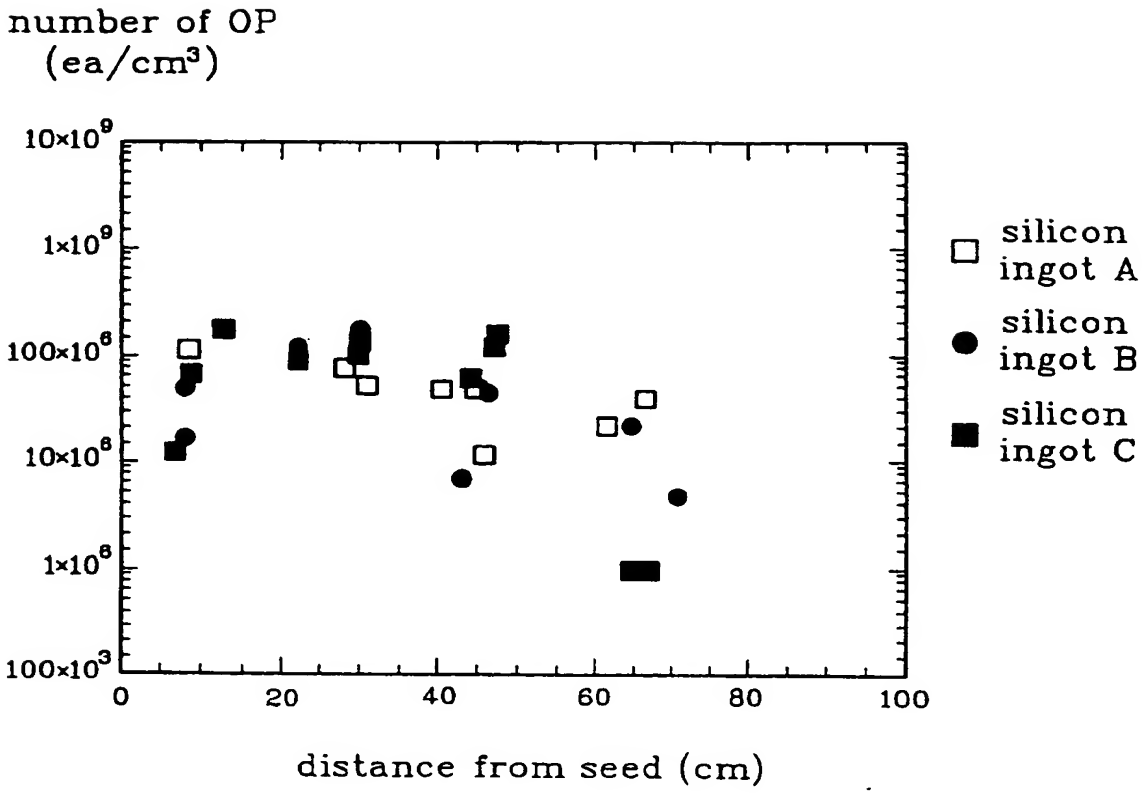


FIG. 2
(PRIOR ART)

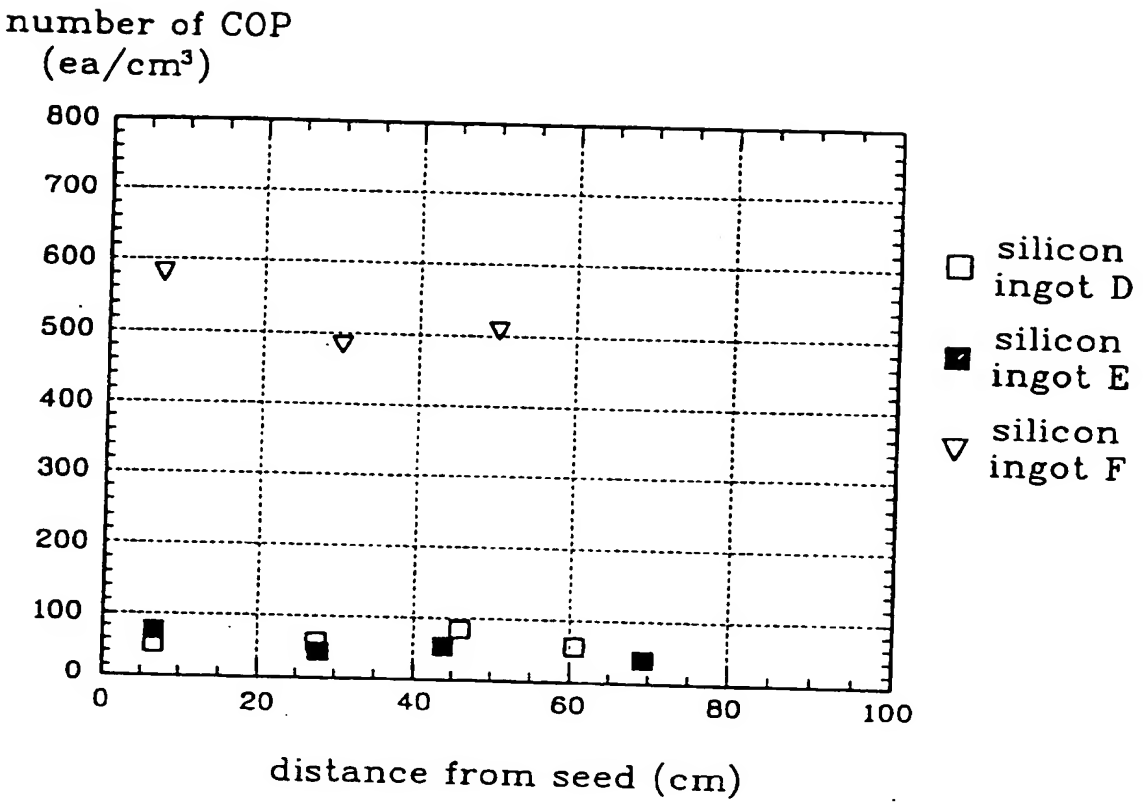


FIG. 3
(PRIOR ART)

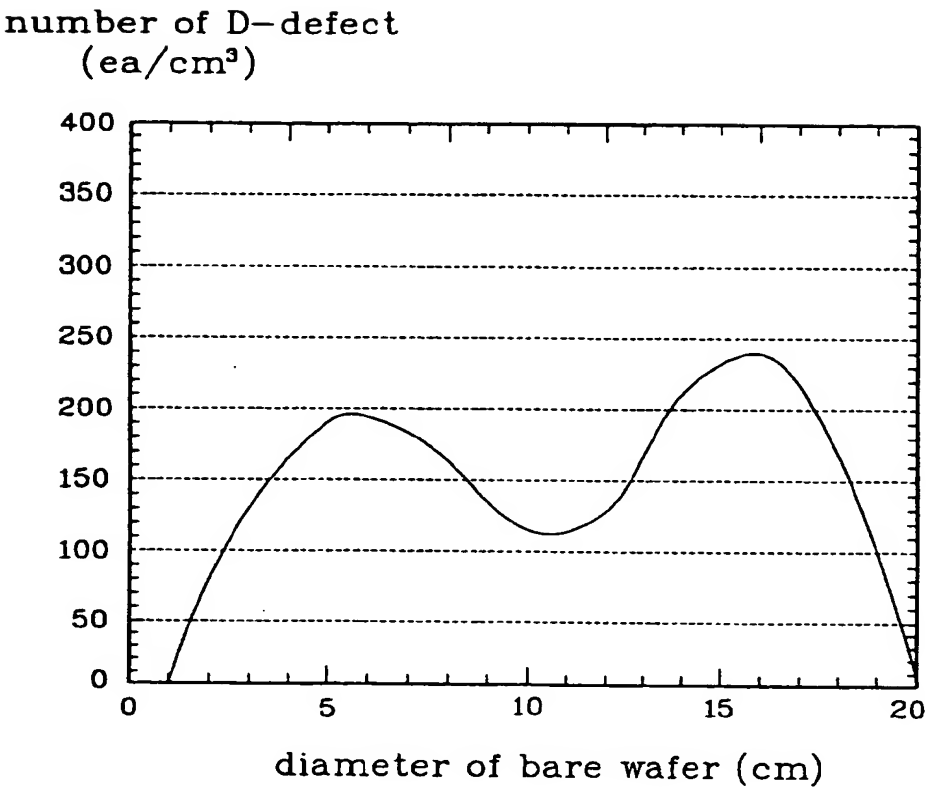


FIG. 4

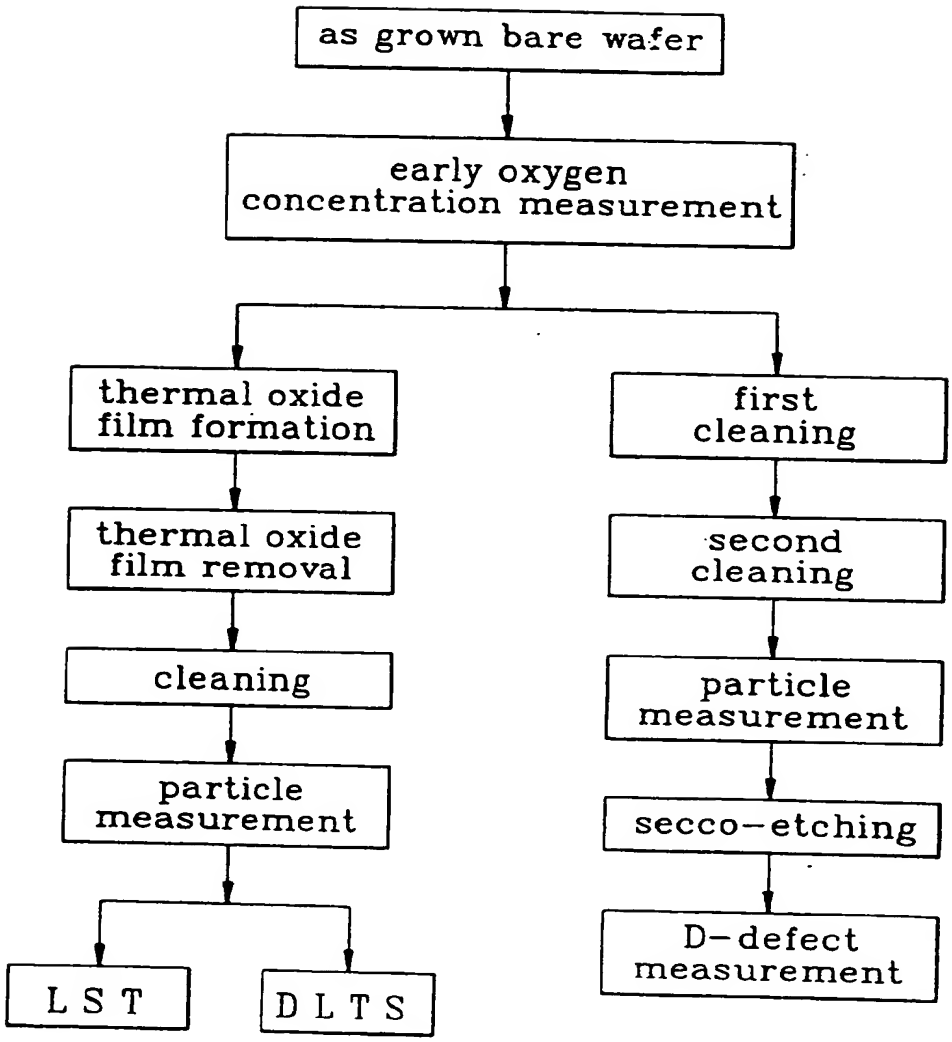

as grown bare wafer
early oxygen concentration measurement
thermal oxide film formation
thermal oxide film removal
cleaning
particle measurement
L S T
D L T S
first cleaning
second cleaning
particle measurement
secco-etching
D-defect measurement

FIG. 5

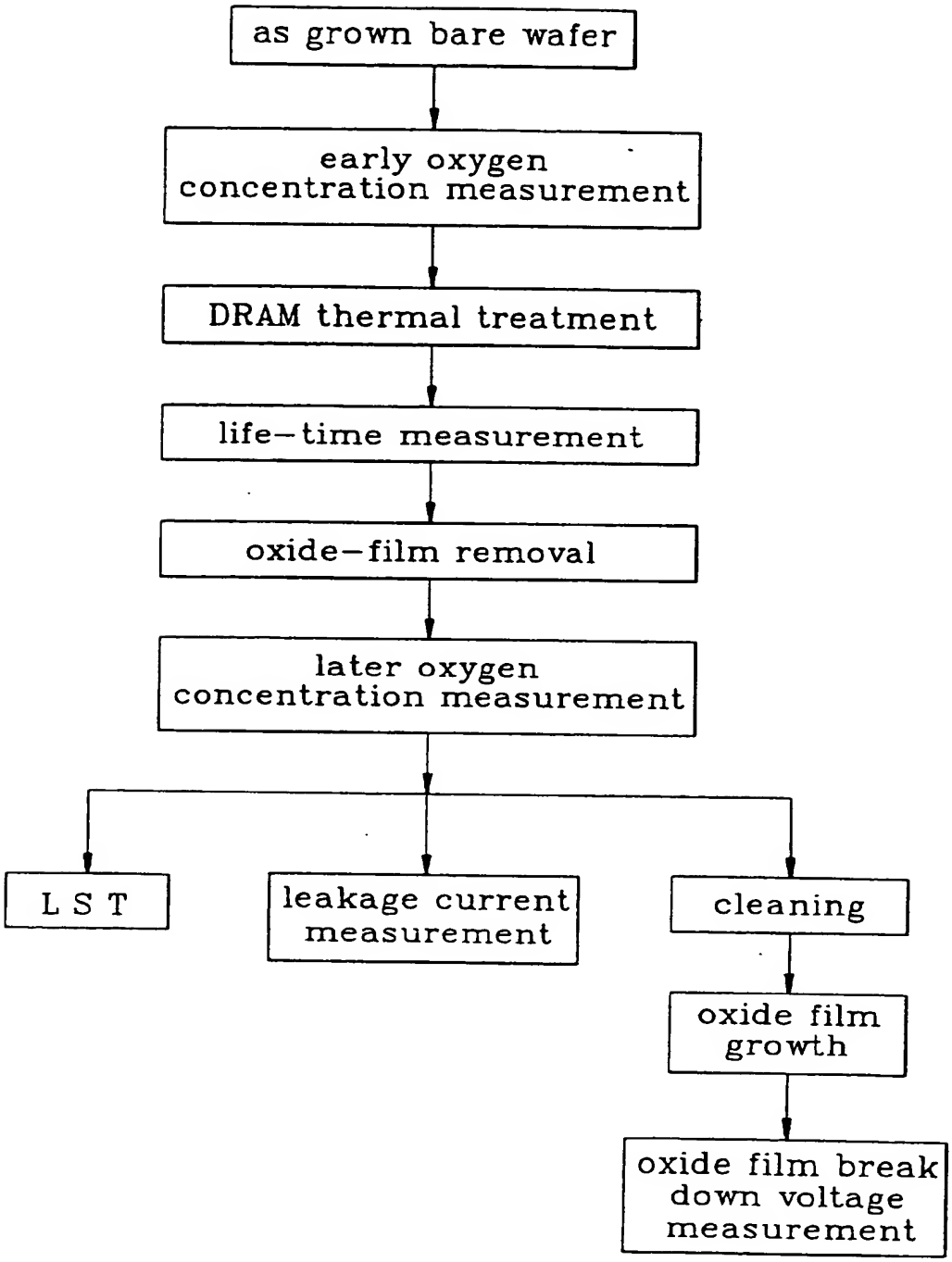

as grown bare wafer
early oxygen concentration measurement
DRAM thermal treatment
life-time measurement
oxide-film removal
later oxygen concentration measurement
L S T
leakage current measurement
cleaning
oxide film growth
oxide film break down voltage measurement

FIG. 6

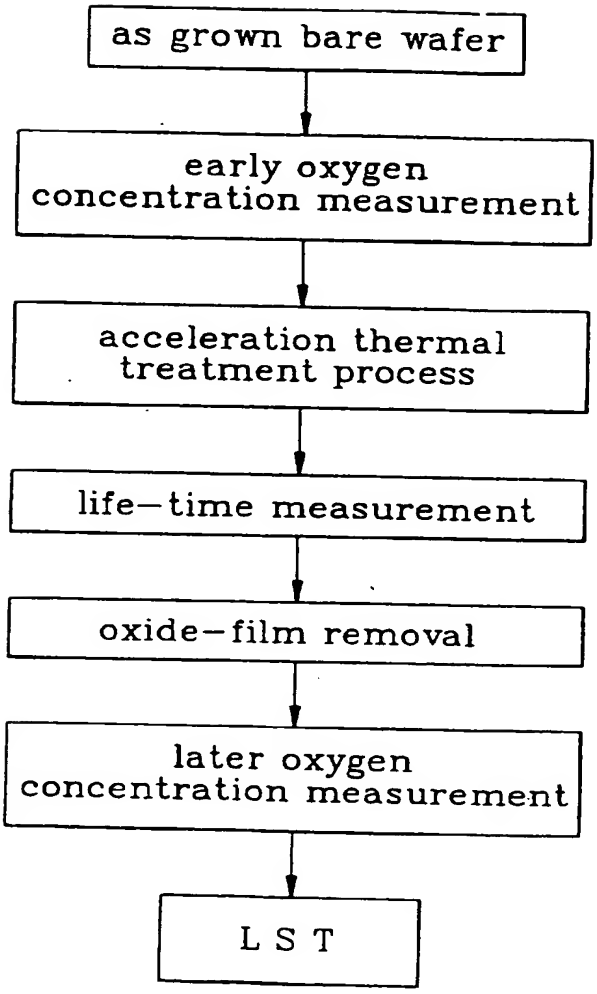

as grown bare wafer
early oxygen concentration measurement
acceleration thermal treatment process
life-time measurement
oxide-film removal
later oxygen concentration measurement
L S T

FIG. 7

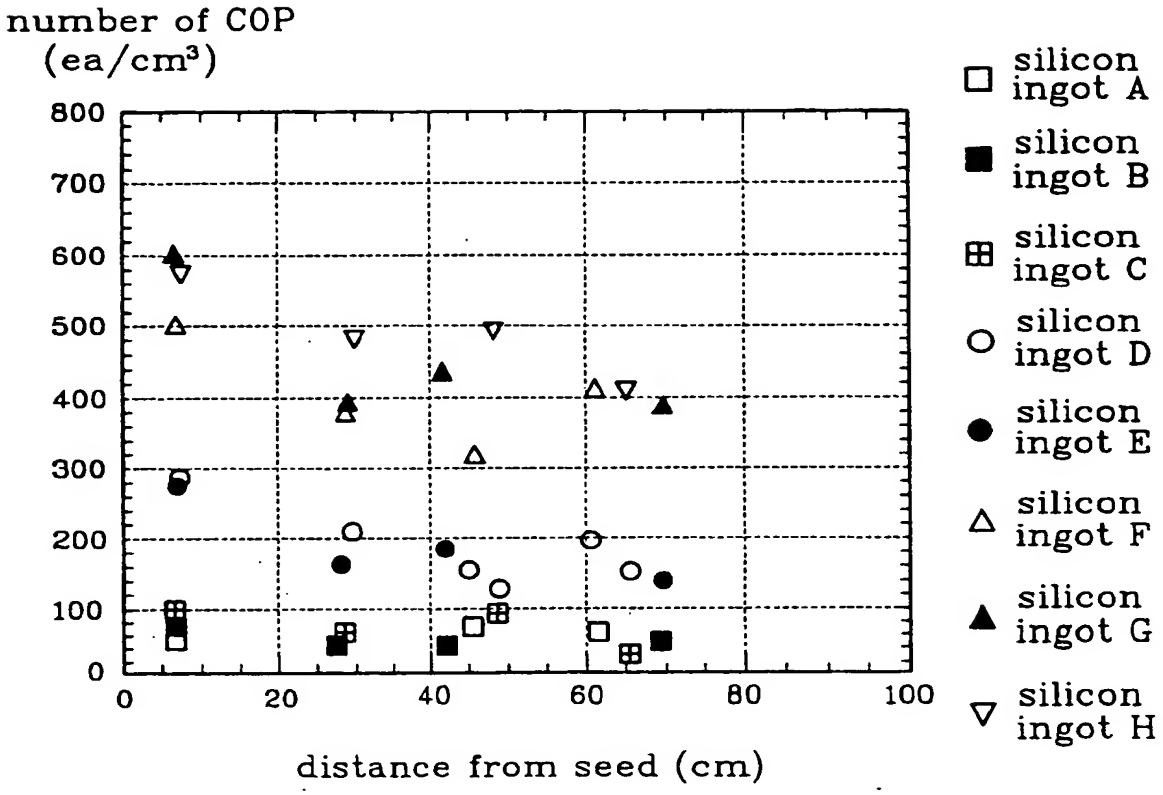

number of COP
(ea/cm³)
800
700
600
500
400
300
200
100
0
0
20
40
60
80
100
distance from seed (cm)
silicon ingot A
silicon ingot B
silicon ingot C
silicon ingot D
silicon ingot E
silicon ingot F
silicon ingot G
silicon ingot H

FIG. 8

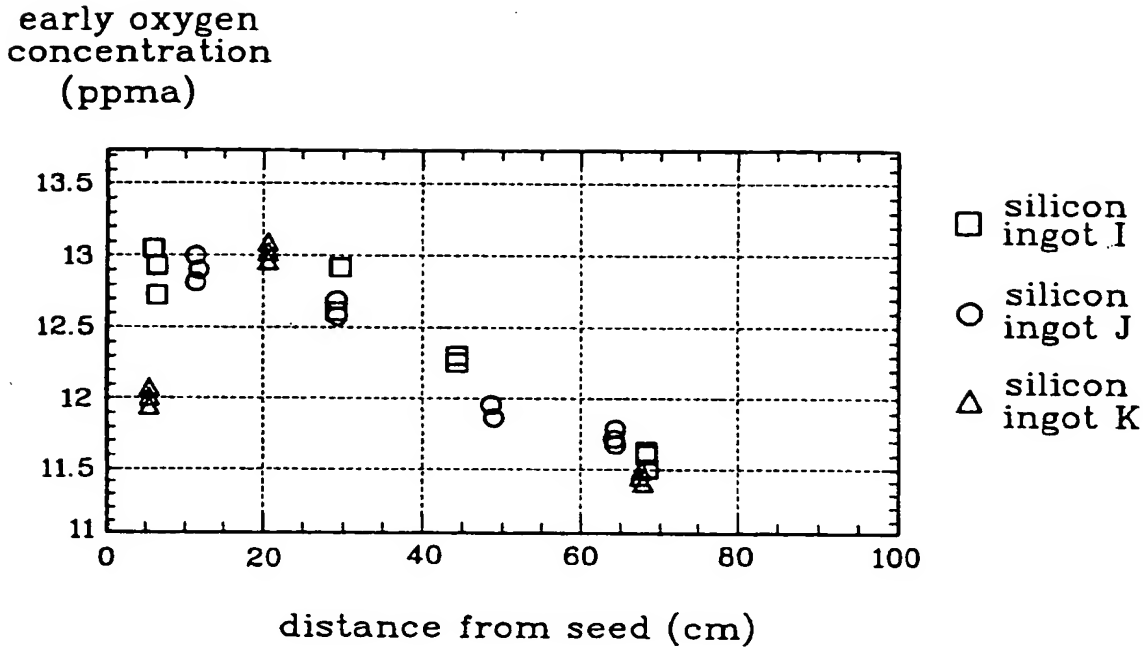

early oxygen concentration (ppma)
13.5
13
12.5
12
11.5
11
0
20
40
60
80
100
distance from seed (cm)
silicon ingot I
silicon ingot J
silicon ingot K

FIG. 9

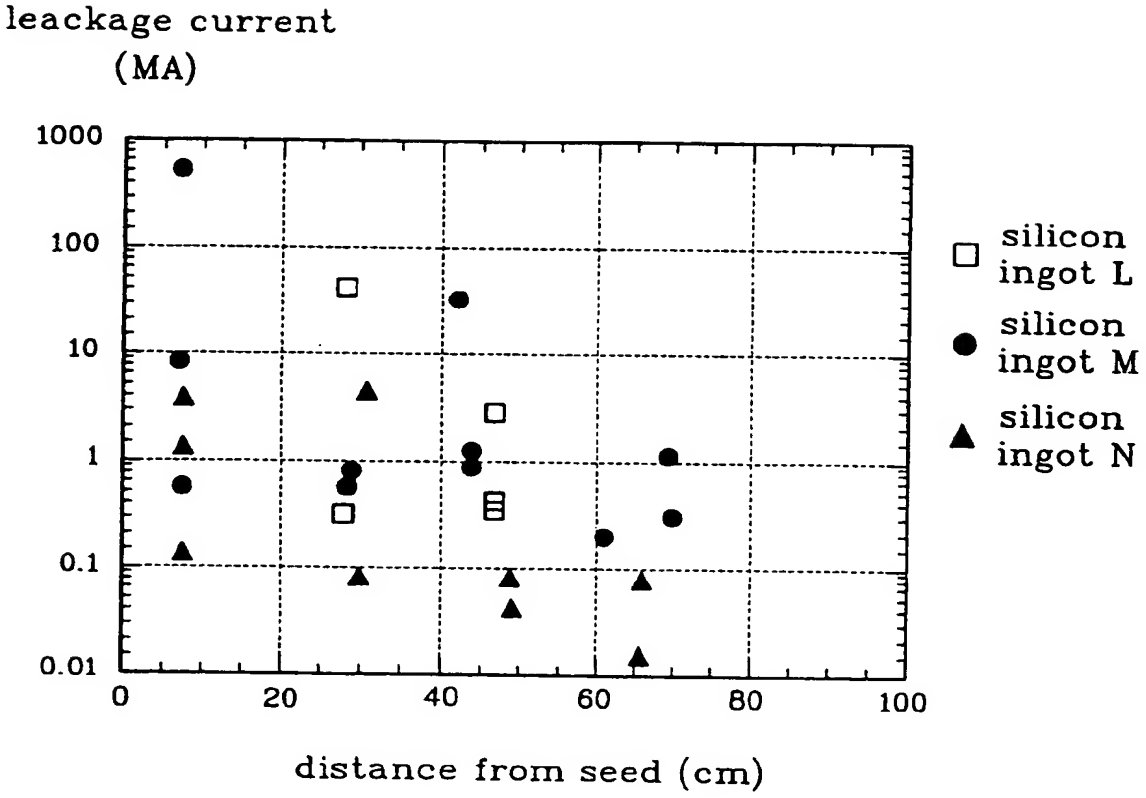

leackage current
(MA)
1000
100
10
1
0.1
0.01
0
20
40
60
80
100
distance from seed (cm)
silicon ingot L
silicon ingot M
silicon ingot N

FIG. 10

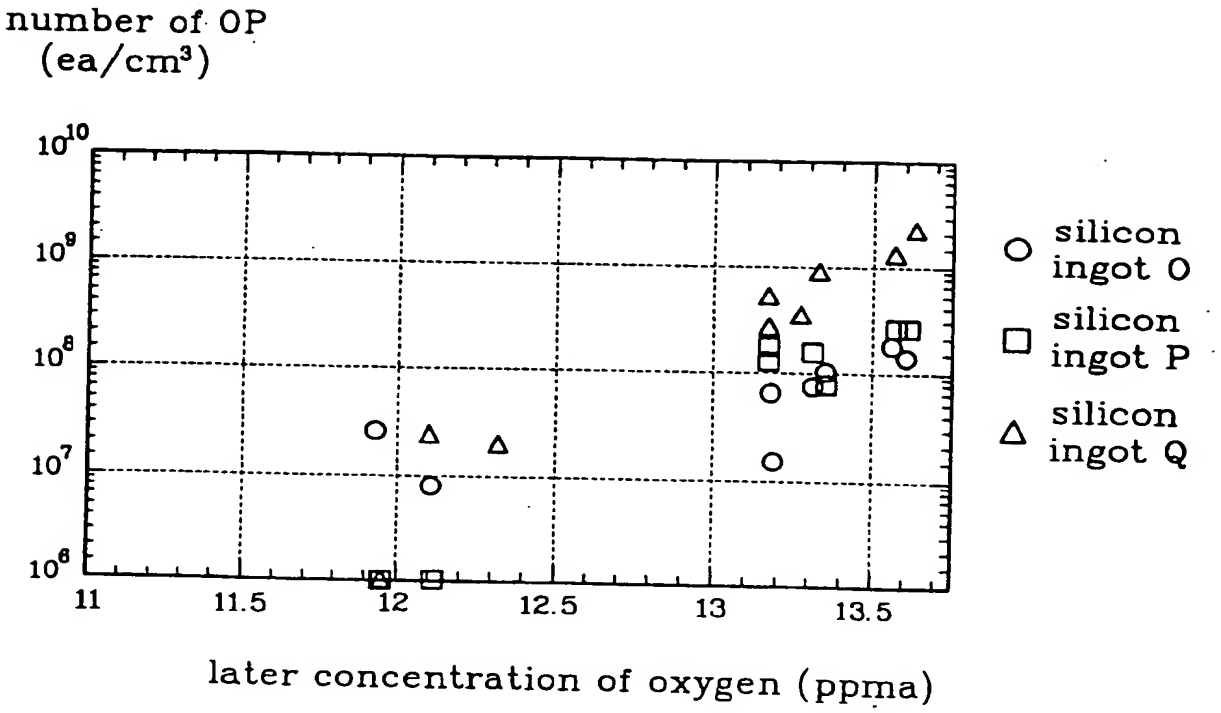

number of OP
(ea/cm³)
10¹⁰
10⁹
10⁸
10⁷
10⁶
11
11.5
12
12.5
13
13.5
later concentration of oxygen (ppma)
silicon ingot O
silicon ingot P
silicon ingot Q

FIG. 11

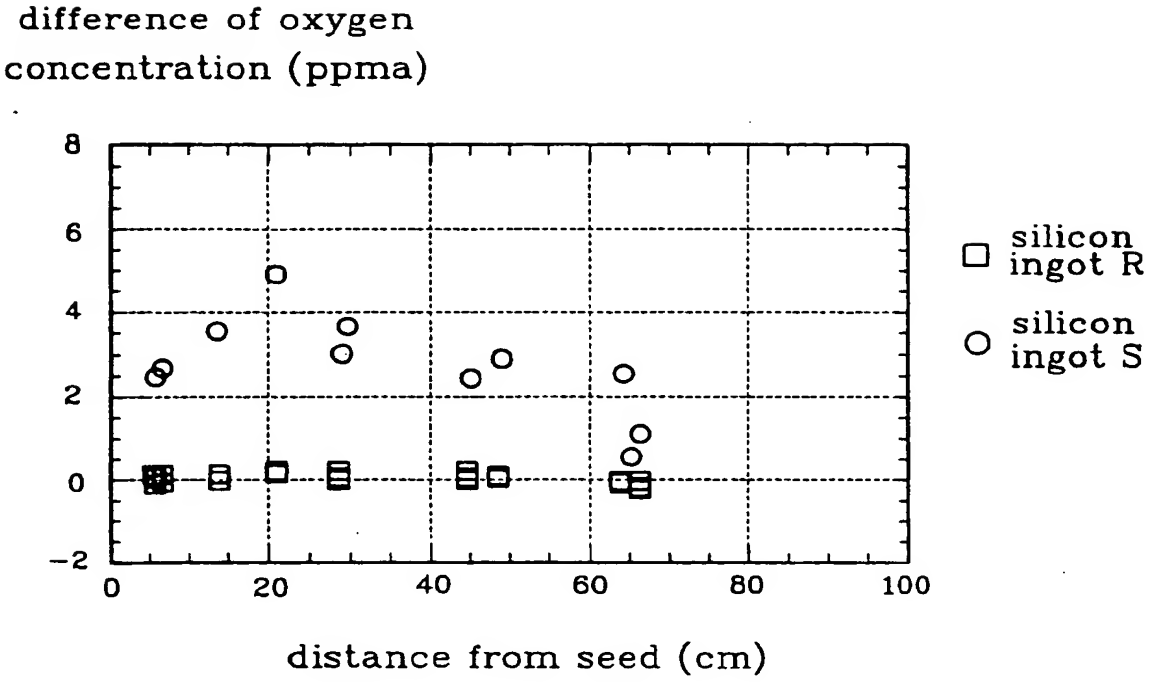

difference of oxygen
concentration (ppma)
8
6
4
2
0
−2
0
20
40
60
80
100
distance from seed (cm)
silicon ingot R
silicon ingot S

FIG. 12

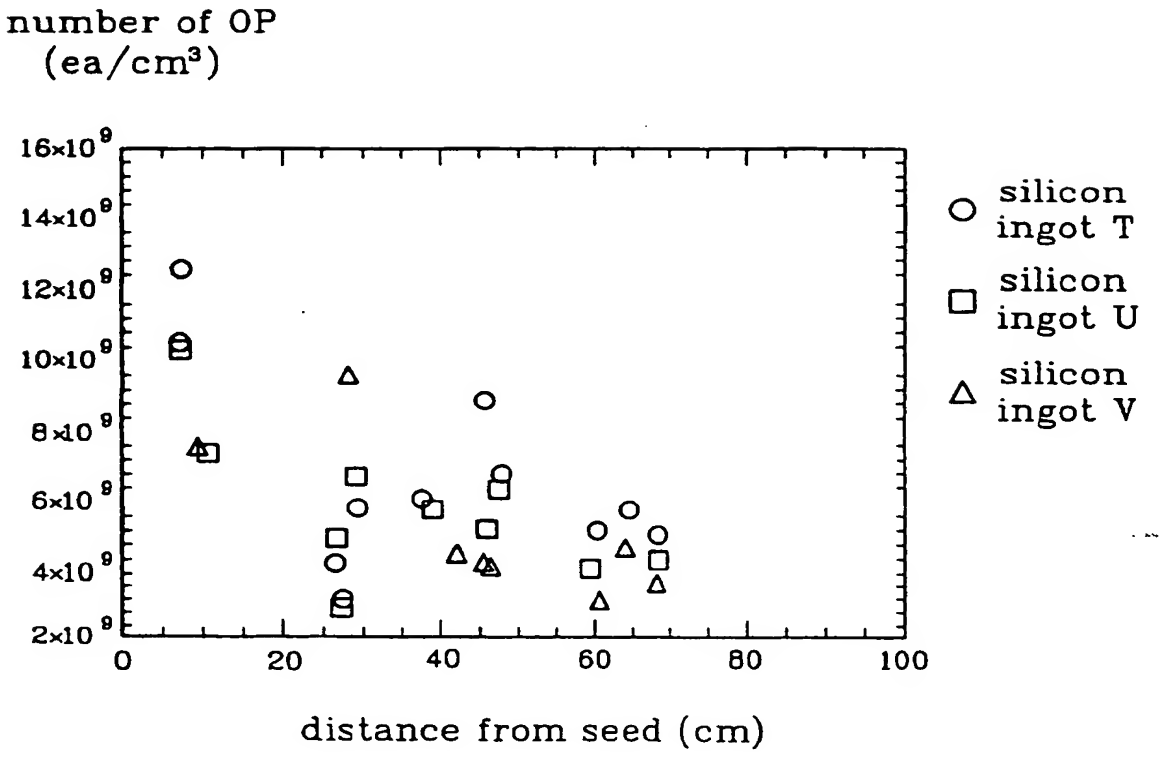

number of OP
(ea/cm³)
16×10⁹
14×10⁹
12×10⁹
10×10⁹
8×10⁹
6×10⁹
4×10⁹
2×10⁹
0
20
40
60
80
100
distance from seed (cm)
silicon ingot T
silicon ingot U
silicon ingot V

FIG. 13

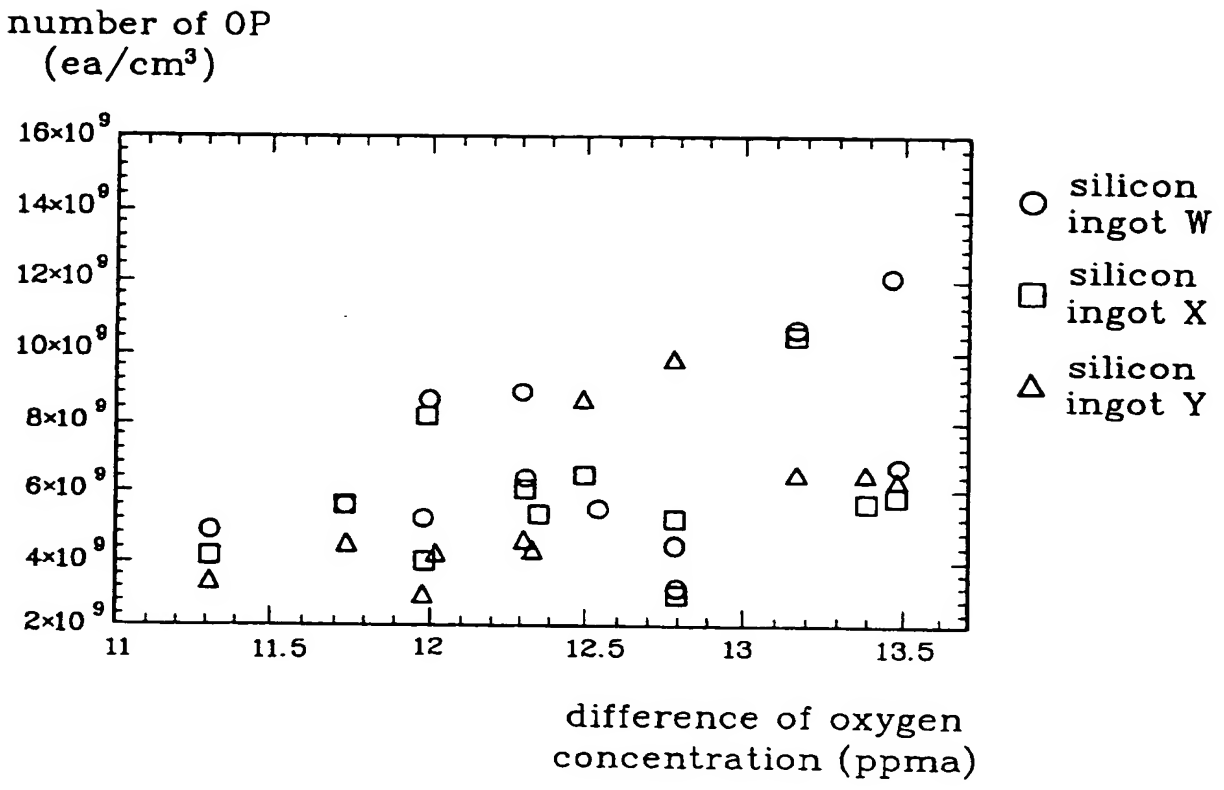
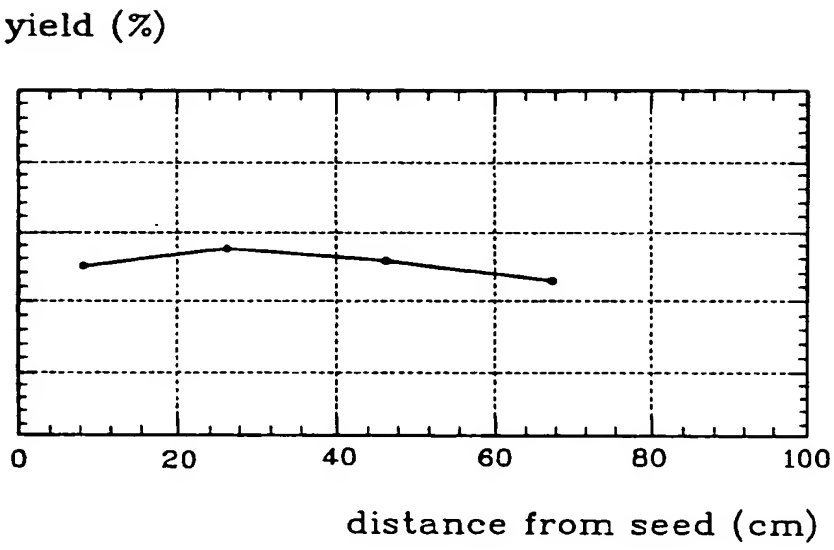

number of OP
(ea/cm³)
16×10⁹
14×10⁹
12×10⁹
10×10⁹
8×10⁹
6×10⁹
4×10⁹
2×10⁹
11
11.5
12
12.5
13
13.5
difference of oxygen
concentration (ppma)
silicon ingot W
silicon ingot X
silicon ingot Y

FIG. 14



METHOD OF ANALYZING A SEMICONDUCTOR INGOT

The present invention relates to a method of analyzing a semiconductor ingot, and more particularly, a method of more easily analyzing the crystal defects on the surface of a bare wafer formed by single crystal growth.

Generally, bare wafers for manufacturing semiconductor devices are prepared in such a manner that poly-crystal silicon is produced inside an electric furnace by reduction using silicon and silicon dioxide as main source, and cork and wood as auxiliary source, and then it is refined

Then, a single crystal ingot, its one end called seed, and its the other end called tail, is formed by Czochralski crystal growth and Float zone crystal growth, and by a subsequent process, one end of the single crystal ingot undergoes grinding so as to form a Flat zone region of bare wafer, and the single crystal ingot is cut for round discs.

The bare wafers for use in a semiconductor device fabrication process are prepared when the surfaces of the above-mentioned round discs are ground.

In the Czochralski crystal growth, poly-crystal silicon is melted in a crystal growth crucible at a temperature of about 1415 ^{0}C, and if the crystal growth crucible is rotated, an arm having crystal seed of single crystalline silicon attached thereon slowly falls down so as to touch the crystal seed on the surface of the melted silicon.

Accordingly, when the crystal seed contacts the melted silicon, the arm is slowly moved upwards. The crystal seed and some of its contacting melted silicon moves upward with the arm's upward movement. The crystal seed keeps growing by the cooling of the melted silicon around the contact surface of the two substances, and the crystallization thereof so that a single crystal ingot having the same crystal structure as that of the crystal seed is formed.

Inside the crystal growth chamber of the Float zone crystal growth, there are an upper chuck and a lower chuck with a single crystal silicon seed fixed thereon. A poly crystal silicon ingot is inserted between the upper chuck and the lower chuck so that the poly crystal silicon ingot and the seed crystal contact, and a movable induced heating coil heats the poly crystal silicon ingot.

When a specific voltage is applied to the induced heating coil, the heat generated from the induced heating coil is transferred to the contact surface of the polycrystal silicon ingot and the crystal seed so as to start to melt the poly crystal silicon ingot.

The induced heating coil moves upwards. The contact surface of the melted poly crystal silicon ingot and the crystal seed first cools down, and by the crystallization due to the cooling, the crystal seed slowly grows so that a single crystal silicon ingot having the same crystal structure as that of crystal seed is formed.

Inside the bare wafer prepared by the Czochralski crystal growth and Float zone crystal growth, D-defect is formed with an empty space of octahedron shape for various reasons such as temperature difference

inside the crystal growth crucible, and COP (Crystal Originated Particles) are formed on the surface of the bare wafers with grooves because some parts of the D-defects are cut or exposed while the upper side of the bare wafer is polished. The D-defect and COP cause reduction of the break down voltage of the oxide film formed on the bare wafer in the following process.

Especially, in the Czochralski crystal growth, OP (oxygen precipitates) are formed inside the bare wafer because early oxygen element is included in the melted poly crystal silicon in the crystal growth crucible and metallic contaminants exist inside the bare wafer because heavy metallic contaminants are included in the melted poly crystal silicon in the crystal growth crucible. The OP and the metallic contaminants are the source of current leakage when power is applied to the semiconductor devices formed on the bare wafers.

Meanwhile, the above crystal defects are generated for various reasons during the ingot growth process, but precise analysis of the morphology, distribution, and density is not made, and therefore, the production yield is decreased because the above crystal defects keep affecting the semiconductor wafers in the following semiconductor device fabrication process.

However, there is no method to precisely analyze the defects on the surface of bare wafers, which greatly affect the production yield of the semiconductor devices, and there is a great demand for the development of an analysis method for the crystal defects.

The present invention is directed to providing a method of analyzing a semiconductor ingot which allows precise analyzing of the

distribution or density of defects existing on the surface of bare wafers by carrying out various analyzing steps on a plurality of bare wafers in a semiconductor device fabrication process.

To achieve this and other advantages and in accordance with the purpose of the present invention, a method of analyzing a semiconductor ingot comprises the steps of:

a) sampling wafers with respect to their position in said ingot after forming wafers from a plurality of ingots formed under the same crystal growth conditions ; b) analyzing the crystal defects of the wafers in as-grown state after selecting a part of said sampled as-grown wafers with respect to each position in the ingots ; c) selecting some other wafers among the sampled as-grown wafers with respect to the positions in the ingots, carrying out a thermal treatment process under the same temperature conditions on said wafers as the thermal treatment process of a semiconductor device fabrication process and analyzing the crystal defects of the wafers; d) selecting some other wafers among the as-grown sampled wafers with respect to the positions in the ingots, carrying out an acceleration thermal treatment on the wafers, and analyzing the crystal defects, and e) estimating the state of the crystal defects with respect to the positions in ingots based on the above analysis results.

The analysis is carried out on silicon ingots by Czochralski crystal growth, and the important crystal defects analyzed are OP (oxygen precipitate), COP (Crystal Originated Particle), D-defect, and heavy metal defects. The analysis steps of the crystal defects include the distribution and the density measurement of each crystal defect in the wafers.

The measurement of early oxygen concentration in the sampled wafers is carried out before each analysis step and preferably the results are compared with the results measured in the following measurement of the late oxygen concentration for the analysis of the crystal defects.

Meanwhile, the sampled wafers in the step of analyzing the crystal defects in the as-grown state are cleaned and the COP is measured by using a particle counter and an Atomic Focus Microscope.

After analyzing the COP, the wafers are seco-etched, and the D-defect of the wafers is measured by using a Microscope and scanning.

In the step of analyzing the crystal defects in the as-grown state, the COP is detected after forming thermal oxide film on the other sampled bare wafers, removing it and cleaning the bare wafers. Then, the OP is measured by using an LST (Laser Scattering Tomography) method, and the heavy metal is detected by using a DLTS (Deep Level Transient Spectrometer) method.

In the step of analyzing the crystal defects after a thermal treatment under the same temperature conditions on the wafers as the thermal treatment process of a semiconductor device fabrication process, the OP is measured by removing the oxide film formed on the wafers after the thermal treatment, and selecting some wafers and by using the LST method. In this step, the leakage current is measured by selecting some other wafers after removing the oxide film formed on the wafers by the above thermal treatment. In this step, after the thermal treatment, removing the oxide film formed on the wafers, selecting the other wafers, cleaning and growing the oxide film on the wafers, the oxide film breakdown voltage is measured. In this step, after the above thermal

treatment process, and removing the oxide film formed on the wafers, the late oxygen concentration is measured. In this step, the crystal defects can be measured after carrying out a thermal treatment, measuring life time, and removing the oxide film formed on the wafers.

In the step of analyzing the crystal defects after the acceleration thermal treatment, the OP is measured after the acceleration thermal treatment, removing the oxide film formed on the wafers, and by using the LST method. Or, after removing the oxide film, and before measuring the OP, the late oxygen concentration is measured. Or, after the acceleration thermal treatment process, measuring life time, and removing the oxide film formed on the wafers, the crystal defects can be measured.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

An embodiment of the present invention will now be described by way of example only with reference to the accompanying drawings in which:

Fig. 1 is a graphical representation showing the OP-distribution of seed-to-tail ingots formed by Czochralski crystal growth;

Fig. 2 is a graphical representation showing the COP-distribution of seed-to-tail ingots formed by Czochralski;

Fig. 3 is a graphical representation showing the D-defect distribution from one end of a bare wafer to its opposite end, the bare wafer being formed by cutting an ingot grown by Czochralski;

Fig. 4 is a processing chart for analyzing the defects on as-grown bare wafers according to one embodiment of the present invention;

Fig. 5 is a processing chart for analyzing the defects on bare wafers on which the same thermal treatment with a DRAM (Dynamic Random Access Memory) thermal treatment is carried out according to one embodiment of the present invention;

Fig. 6 is a processing chart for analyzing the defects on bare wafers passing through an acceleration thermal treatment according to one embodiment of the present invention;

Fig. 7 is a graphical representation showing the distribution of seed-to-tail COP of ingots by the processing chart of Fig. 4;

Fig. 8 is a graphical representation showing the distribution of early oxygen concentration in seed-to-tail ingots by the processing chart of Fig. 4;

Fig. 9 is a graphical representation showing leakage current measured on the bare wafers prepared by cutting an ingot from its seed to its tail by the processing chart of Fig. 5;

Fig. 10 is a graphical representation showing the concentration of late oxygen existing on the bare wafers prepared by cutting an

ingot from its seed to its tail and the leakage current measured on the bare wafers by the processing chart of Fig. 5;

Fig. 11 is a graphical representation showing the difference between the early concentration and the later concentration of the oxygen existing on the bare wafers prepared by cutting an ingot from its seed to its tail by the processing chart of Fig. 6 of the present invention;

Fig. 12 is a graphical representation showing the number of the OP on the bare wafers prepared by cutting an ingot from its seed to its tail according to the processing chart of Fig. 6;

Fig. 13 is a graphical representation showing the OP number and the difference between the early concentration and the later concentration of the oxygen existing on the bare wafers prepared by cutting an ingot from its seed to its tail according to the processing chart of Fig. 6; and

Fig. 14 is a graphical representation showing the yield of the semiconductor devices formed on the bare wafers prepared by cutting an ingot grown by single crystal growth.

An ingot is cut from its seed to its tail and the crystal defects of the bare wafers such as OP, COP, and D-defects are analyzed.

Fig. 1 is a graphical representation showing the OP-distribution of seed-to-tail wafers cut from ingots formed by Czochralski crystal growth, Fig. 2 is a graphical representation showing the COP-distribution of seed-to-tail wafers cut from ingots formed by Czochralski, and Fig. 3 is a

graphical representation showing the D-defect distribution from one end of a bare wafer to its opposite end, wherein the bare wafer is formed by cutting an ingot grown by Czochralski.

Referring now to Fig. 1, a plurality of wafers are prepared by thin cutting an ingot grown by Czochralski crystal growth from its seed to its tail, the number of OP is measured by using an LST method, and the analysis for the OP distribution is done. As shown in Fig. 1, the distribution and the number of OP differ with respect to the positions in the ingot.

The number of OP is measured by the LST method in which the tomograph of the defect is taken by using scattered laser light.

Referring to Fig. 2, a plurality of wafers are prepared by thin cutting the ingot grown by Czochralski crystal growth from its seed to its tail, the COP distribution is analyzed by using a particle counter and Atomic Focus Microscope and the analysis for the COP number is done. The number of COP is decreased further from the seed to the tail of the ingot as shown in Fig. 2.

The number of COP is measured by irradiating laser light on the bare wafer and by using a particle counter, and detecting the scattered light from the wafer. The distribution of COP is analyzed by using an Atomic Focus Microscope and scanning the surface of the bare wafer.

Referring to Fig. 3, the distribution of D-defect is analyzed for the bare wafers formed by thin cutting the ingot grown by the Czochralski crystal growth method. The analysis for the number of D-defect is done, and as shown in Fig. 3, the number of D-defect existing on the edge of

the bare wafers is relatively lower than that of D-defect on the center of the bare wafers.

The analysis of the D-defect is done as follows. First, the bare wafers are Secco etched by putting them into a container having Secco etching solution comprising HF, $K_2Cr_2O_3$, and deionized water and maintaining a certain temperature. The D-defect existing in the bare wafers is etched and a flow pattern is formed. The flow pattern is scanned by using the Microscope, and the number of D-defect on the bare wafers is measured so that the distribution of D-defect is detected.

The numbers of OP and COP of the bare wafers formed by cutting the ingot of the Fig. 1 to Fig. 3 are different with respect to the positions in the ingot. The distribution of the D-defect is different with respect to the position in the bare wafers. Therefore, the semiconductor devices formed on the bare wafers have a different probability for malfunctioning with respect to the positions of the bare wafers. That is, some semiconductor devices from a bare wafer can function well and those from a different bare wafer can ill-function.

Fig. 4 is a processing chart for analyzing the defects on the as-grown bare wafers according to one embodiment of the present invention.

Referring now to Fig. 4, six single crystal ingots formed by conducting single crystal growth processes three times repeatedly under the common growth conditions in two single crystal growth furnaces are cut and the samples are selected from four positions, that is, seed, center 1, center 2, and tail, and two bare wafers from each position. That is ,

48 pieces of as-grown bare wafers are sampled. In order to standardize the analysis results, more samples can be selected.

For the sampled 48 pieces of bare wafers, the analysis of the early oxygen concentration is done to measure the concentration of the oxygen existing on the crystal of the bare wafer which may provide the causes of the mal-functioning of the semiconductor devices as OP in the semiconductor devices fabrication process. The measurement of the early oxygen concentration is conducted by an FT-IR (Fourier Transfer Infrared) method in which the infrared rays irradiate the bare wafers and the oxygen concentration is analyzed according to the light reflected from the bare wafers.

Then, 24 pieces of samples are selected from the bare wafers for which the early concentration of oxygen has been measured, and a first cleaning process to remove the contaminants existing on the bare wafers is done for about 2 hours by putting the bare wafers in a container having a cleaning solution comprising hydrogen peroxide, deionized water, and ammonium hydroxide, etc.

Then, after the first cleaning process to remove the contaminants on the bare wafers, a second cleaning process is used to remove contaminants which reattach on the bare wafers.

Then, the number of COP existing on the bare wafers undergoing the second cleaning process is measured by using an Atomic Focus microscope.

Then, after secco-etching the bare wafers, the number of D-defect existing on the bare wafers is measured by using a microscope.

For the other 24 pieces of bare wafers for which early concentration of the oxygen has been measured, a thermal treatment is done so as to form a thin thermal oxide film on the bare wafers, and remove the thermal oxide film. Depending on the formation of the thermal oxide film, the defects existing on the bare wafers are grown to a suitable size for the analysis process.

A bare wafer whose thin thermal oxide film is removed is cleaned by using a cleaning solution comprising hydrogen peroxide, deionized water, and ammonium hydroxide appropriately mixed.

Then, the number of COP existing on the bare wafer is measured by using a particle counter, and the distribution of the COP existing on the bare wafer is analyzed by using an Atomic Focus Microscope to scan the defects existing on the bare wafer by the migration of tip.

Then, the number of OP existing on the bare wafer undergoing the above particle measurement process is analyzed by conducting an LST method. Then, the amount of the heavy metal existing on the other bare wafers undergoing the particle measurement process is analyzed by using a DTLS (Deep Level Transient Spectrometer).

The metal contaminants on the bare wafer is analyzed by applying power to the bare wafers and using a DLTS (Deep Level Transient Spectrometer) to measure the excessive current.

As described above, the number of the COP and D-defect existing on the bare wafers cut according to the positions in the ingot formed by single crystal growth, and the distribution of the COP and OP and the

amount of heavy metal existing on the bare wafers after removing the thermal oxide film are achieved.

Fig. 5 is a processing chart for analyzing the defects on the bare wafers on which the same thermal treatment with a DRAM thermal treatment is carried out according to one embodiment of the present invention.

Referring now to Fig. 5, an as-grown bare wafer is sampled, and the early concentration of oxygen existing on the bare wafer is measured. The oxygen existing on the bare wafer is formed as oxygen precipitates inside the bare wafer in the semiconductor device fabrication process, and provides the reason for the mal-funcioning of semiconductor devices. The early concentration of the oxygen is analyzed by FT-IR used to irradiate infrared rays on the bare wafers, and measure the oxygen concentration according to the reflection of the infrared rays reflected from the bare wafers.

Then, the same DRAM thermal treatment process with the same thermal treatment process repeatedly conducted for 16M DRAM is carried out on the bare wafer for which early oxygen concentration has been measured.

Accordingly, the defects existing on the bare wafer are greatly grown and a thin thermal oxide film is formed on the bare wafer.

After injecting contaminants, that is, carriers on the bare wafers, life time is measured in order to analyze most of the crystal defects on the bare wafers, wherein life time is shown to be short because the injected carriers are recombined by the crystal defectiveness, such as contaminants

inside the crystal, ion crystal defects, and the distortion of the surface, etc. and extinguished.

Then, after removing the thin oxide film formed on the bare wafers during the DRAM thermal treatment process, the late oxygen concentration existing on the bare wafer is measured. Accordingly, by detecting the concentration of the oxygen accumulated on a bare wafer from the difference between the early concentration and the late concentration of the oxygen, the amount of the oxygen precipitate solidified on the bare wafer during the 16 M DRAM thermal treatment process can be measured.

Then, some of the bare wafers for which the late concentration of oxygen has been measured are sampled and the number of OP existing thereon is detected by using an LST method.

After forming a thin oxide film on the bare wafer for which the late concentration of the oxygen has been detected, the process of detecting the current leakage is carried out.

Finally, after sampling another bare wafer for which the late concentration of oxygen has been detected, cleaning it by using the cleaning solution, and forming a thin oxide film on the bare wafer, the breakdown voltage of the oxide film is measured.

Accordingly, the change of the defects is detected during the 16 M DRAM formation process. As shown in Fig. 9, the leakage current detected on the bare wafer with respect to its position in the ingot is achieved and as shown in Fig. 10, the number of OP and the late concentration of oxygen detected on the bare wafer are achieved.

Fig. 6 is a processing chart for analyzing the defects on the bare wafers passing through an acceleration thermal treatment according to one embodiment of the present invention. Referring now to Fig. 6, after sampling as-grown bare wafers, and by using an FT-IR method, the early concentration of oxygen existing on a bare wafer is measured.

The acceleration thermal treatment process is carried out to apply heat so that the D-defects and the OP formed during the single crystal growth process can be determined. In this stage, a thin oxide film is formed on the bare wafer.

Life time, the average time until the carriers injected on the bare wafer are extinguished, is measured.

Next, the oxide film formed on the bare wafer during the acceleration thermal treatment process is removed.

Next, the late concentration of the oxygen existing on the bare wafer whose oxide film is removed is measured. By determining the concentration of the accumulated oxygen by subtracting the late concentration of the oxygen from its early concentration, the amount of the oxygen precipitates accumulated on the bare wafer during the acceleration thermal treatment is detected.

Finally, the number of the OP existing on the bare wafer is determined by using an LST method.

Accordingly, the change of the defects is analyzed during the acceleration thermal treatment process. As shown in Fig. 11, the

concentration of the accumulated oxygen existing on the bare wafers with respect to their positions in the ingot, and as shown in Fig. 12, the number of the OP on the bare wafers with respect to their positions in the ingot is achieved. In addition, the number of the OP with respect to the concentration of the accumulated oxygen is achieved.

According to the results from analyzing the production yield after forming 16M DRAM on the bare wafers not undergoing the above analysis process, the region having more defects has a lower production yield as shown in Fig. 14.

Therefore various analysis processes can be made by sampling a plurality of bare wafers with respect to their positions in the ingot, and precisely analyzing the defects on the bare wafers so as to confirm their connection with the production yield of the semiconductor devices results in improvement of the production yield.

Still further, while the present invention has been described in detail, it should be understood that various changes, substitutions and alterations can be made hereto without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS

1. A method of analyzing the crystal defects on a semiconductor ingot formed by a single crystal growth method, the method comprising the steps of:

a) sampling wafers with respect to their positions in said ingot after forming wafers from a plurality of ingots formed under the same crystal growth conditions;

b) analyzing the crystal defects of the wafers in as-grown state after selecting a part of said sampled as-grown wafers with respect to each position in said ingots;

c) selecting some other wafers from among said sampled wafers with respect to the positions in said ingots, carrying out a thermal treatment process on said wafers under the same temperature conditions as the thermal treatment process of a semiconductor device fabrication process and analyzing the crystal defects;

d) selecting some other wafers from among said sampled wafers with respect to the positions in said ingots, carrying out an acceleration thermal treatment on said wafers, and analyzing the crystal defects of the wafers; and

e) estimating the state of the crystal defects with respect to the positions in the ingots based on the above analysis results.

2. The method of analyzing the crystal defects on a semiconductor ingot as claimed in claim 1, wherein said ingot is a silicon ingot grown by Czochralski growth method.

3. The method of analyzing the crystal defects on a semiconductor ingot as claimed in claim 1 or claim 2, wherein the analyzed crystal defects include OP (Oxygen Precipitate), COP (Crystal Originated Particle), D-defect and heavy metal defects.

4. The method of analyzing the crystal defects on a semiconductor ingot as claimed in any preceding claim, wherein each step of analyzing includes the measurement of the distribution and the density of each crystal defect in said wafers.

5. The method of analyzing the crystal defects on a semiconductor ingot as claimed in any preceding claim, wherein measurement of early oxygen concentration for said sampled wafers is carried out before each analysis step.

6. The method of analyzing the crystal defects on a semiconductor ingot as claimed in any preceding claim, wherein in said b) step of analyzing the crystal defects of said wafers in as-grown state, COP is detected after cleaning some of said sampled wafers.

7. The method of analyzing the crystal defects on a semiconductor ingot as claimed in claim 6, wherein analysis of said COP is carried out by using a particle counter and an atomic focus microscope.

8. The method of analyzing the crystal defects on a semiconductor ingot as claimed in claim 6 or claim 7, wherein analysis of D-defect is carried out after secco-etching said wafers after analyzing said COP.

9. The method of analyzing the crystal defects on a semiconductor ingot as claimed in claim 8, wherein the analysis of said D-defect is carried out by scanning using a microscope after secco-etching said wafers.

10. The method of analyzing the crystal defects on a semiconductor ingot as claimed in any preceding claim, wherein in said b) step of analyzing crystal defects on said wafers in as-grown state, COP is analyzed by forming an oxide film on some other bare wafers among said sampled ones, removing the film, and cleaning said bare wafers.

11. The method of analyzing the crystal defects on a semiconductor ingot as claimed in claim 10, wherein OP of said bare wafers is analyzed by using an LST (Laser Scattering Tomography) method after analyzing said COP.

12. The method of analyzing the crystal defects on a semiconductor ingot as claimed in claim 10 or claim 11, wherein the amount of the heavy metal of said bare wafers is analyzed by using a DLTS (Deep Level Transient Spectrometer) method after analyzing said COP.

13. The method of analyzing the crystal defects on a semiconductor ingot as claimed in any preceding claim, wherein in said c) step of analyzing the crystal defects, OP is measured by using an LST method after carrying out said thermal treatment process, removing oxide film formed on said bare wafers, and selecting some of said bare wafers.

14. The method of analyzing the crystal defects on a semiconductor ingot as claimed in any preceding claim, wherein in said c) step of analyzing the crystal defects, current leakage is measured by selecting some other wafers after removing the oxide film formed on the wafers by said thermal treatment.

15. The method of analyzing the crystal defects on a semiconductor ingot as claimed in any preceding claim, wherein in said c) step of analyzing the crystal defects, oxide film breakdown voltage is measured by removing oxide film formed on the wafers after said thermal treatment process, selecting some of the other wafers, cleaning and growing an oxide film on said wafers.

16. The method of analyzing the crystal defects on a semiconductor ingot as claimed in any preceding claim, wherein in said C) step of analyzing the crystal defects, late concentration of oxygen is measured after removing oxide film formed on the wafer by said thermal treatment process.

17. The method of analyzing the crystal defects on a semiconductor ingot as claimed in any preceding claim, wherein in said c) step of analyzing the crystal defects, the crystal defects are analyzed after measuring life time after thermal treatment, and removing oxide film formed on the bare wafers.

18. The method of analyzing the crystal defects on a semiconductor ingot as claimed in any preceding claim, wherein in said d) step of analyzing the crystal defects after said acceleration thermal treatment process, OP is measured by removing oxide film formed on the wafers

after said acceleration thermal treatment process, and using an LST method.

19. The method of analyzing the crystal defects on a semiconductor ingot as claimed in claim 18, wherein the late concentration of oxygen is measured before analyzing OP after removing said oxide film.

20. The method of analyzing the crystal defects on the semiconductor ingot as claimed in claim 18 or claim 19, wherein the crystal defects are analyzed after measuring life time after said acceleration thermal treatment process and removing the oxide film formed on the wafers.

21. The method of analyzing a semiconductor ingot substantially as described herein with reference to and as illustrated by the accompanying drawings.

The Patent Office

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Application No: GB 9801252.9
Claims searched: all

Examiner: Martyn Dixon
Date of search: 15 April 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H1K (KMA)

Int Cl (Ed.6): H01L (21/66)

Other: Online: WPI, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	EP 0058337 A	(IBM) see page 8, lines 13 *et seq*	1
A	US 4637123 A	(IBM) see col 5, lines 37 *et seq*	1
A	US 4344815 A	(IBM) see col 6 , lines 51 *et seq*	1

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Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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